CORELIS

ScanPCI

ScanPCI

PCI and CompactPCI Boundary Scan Tester

User's Manual

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User's Manual

Document Part Number 70351, Revision A

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New editions are complete revisions of the manual. Update packages, which are issued between editions, contain additional and replacement pages to be merged into the manual by the customer. The dates on the title page change only when a new edition is published.

A software code may be printed before the date; this indicates the version of the software product at the time the manual or update was issued. Many product updates and fixes do not require manual changes and, conversely, manual corrections may be done without accompanying product changes. Therefore, do not expect a one to one correspondence between product updates and manual updates.

Revision A, September 2003

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TABLE OF CONTENTS

CHAPTER 1 PRODUCT OVERVIEW 1-1

Introduction **1-1**

Required hardware and software **1-3**

CHAPTER 2 SCANPCI INSTALLATION 2-1

Product Components **2-1**

What's on the Disk **2-1**

Connecting the Unit Under Test (UUT) to the ScanPCI **2-2**

Connecting to the Boundary-Scan Controller **2-2**
Target UUT TAP Connections on an External Header 2-2
Target UUT TAP Connections on the PCI Card-edge Connector 2-3

CHAPTER 3 SCANPCI HARDWARE REFERENCE 3-1

Jumper Configuration **3-1**

TAP Connector Pinout **3-2**

Power Indicator LEDs **3-2**

Specifications **3-3**

ScanPCI Operating Characteristics **3-4**

CHAPTER 4 PREPARATION OF TEST INPUT FILES 4-1

Introduction **4-1**

How to Generate Vectors using the ScanPCI **4-1**

CHAPTER 5 TESTING COMPACTPCI CARDS 5-1

Introduction **5-1**

Merging the CompactPCI Adapter and the UUT **5-2**
Step 1 – Starting ScanPlus Merge 5-2
Step 2 – Add the Unit Under Test (UUT) Assembly 5-3
Step 3 – Add the CompactPCI Adapter Assembly 5-7
Step 4 – Add the System Connection File 5-10
Step 5 – Merge the Assemblies 5-12

Modifying the Topology File to Include the ScanPCI **5-14**

CHAPTER 6 EXECUTING SELFTEST WITH SCANPLUS RUNNER 6-1

Infrastructure Test **6-1**

Table of Figures

Figure 1-1. ScanPCI Boundary-Scan Tester *1-1*
Figure 2-1. Connection of the ScanPCI and the Target using Separate TAPs *2-2*
Figure 2-2. UUT Connection Example using Separate TAPs *2-3*
Figure 2-3. Block Diagram of the Connection to a ScanPCI with a Single TAP *2-3*
Figure 2-4. UUT Connection Example Using a Single TAP *2-4*
*Figure 4-1. Example Topology *.top File Before the ScanPCI is Added* *4-2*
*Figure 4-2. Example Topology *.top File After the ScanPCI is Added* *4-2*
Figure 5-1. ScanPlus Merge Main Window *5-2*
Figure 5-2. ScanPlus Merge Main Window with a New Assembly *5-3*
Figure 5-3. ScanPlus Merge Main Window Showing Renamed UUT Assembly *5-4*
Figure 5-4. Assembly Details Window for the UUT Assembly *5-5*
Figure 5-5. Assembly Details Window with Netlist File Row Selected *5-5*
Figure 5-6. UUT Netlist File Selected *5-6*
Figure 5-7. UUT Topology File Selected *5-6*
Figure 5-8. ScanPlus Merge Main Window with a Second Assembly Added *5-7*
Figure 5-9. ScanPlus Merge Main Window Showing Renamed Assembly *5-8*
Figure 5-10. Assembly Details Window *5-9*
Figure 5-11. Assembly Details after Test Step files added *5-9*
Figure 5-12. System Connection File *5-10*
Figure 5-13. System Connection File Browsing Window *5-10*
Figure 5-14. ScanPlus Merge Main Window with System Connection File *5-11*
Figure 5-15. Saving the Merge Plan file *5-12*
Figure 5-16. Confirm File Replace Window *5-12*
Figure 5-17. Merge Status Window Indicating Completion *5-13*
*Figure 5-18. Example Topology *.top File Before the ScanPCI is Added* *5-15*
*Figure 5-19. Example Topology *.top file After the ScanPCI is Added* *5-15*
Figure 6-1. ScanPlus Runner Infrastructure Test *6-2*

Table of Tables

Table 3-2. Files on the Provided Software Disk *2-1*
Table 3-1. Jumper Configuration *3-1*
Table 3-2. TAP Connector Connection List *3-2*
Table 3-3. Signal Level Characteristics *3-3*
Table 3-4. ScanPCI Operating Characteristics *3-4*
Table 5-1. Files Created by the Merge Process *5-14*

Chapter 1
Product Overview

Introduction

The ScanPCI is a boundary-scan based PCI card tester that provides a convenient way to test the PCI card unit under test (UUT) using boundary-scan. An optional adapter is available for testing CompactPCI (cPCI) cards as well. The ScanPCI provides power to the UUT and contains special boundary-scan circuitry to permit interconnect testing of the UUT's PCI/cPCI card-edge connector. It is designed to add boundary-scan control and visibility to PCI connectors that would otherwise be impossible to test or would require expensive wiring adapter harnesses. The ScanPCI is designed to be used with the Corelis ScanPlus family of tools, which are sold separately.

Figure 1-1. ScanPCI Boundary-Scan Tester

The ScanPCI provides the following advantages for testing and programming PCI and CompactPCI (cPCI) cards:

- Enables boundary-scan (JTAG) testing of PCI/cPCI cards
- Extends boundary-scan test coverage and provides easy access to PCI/cPCI edge connectors
- Provides test coverage for the hard-to-test traces between the PCI/cPCI edge connectors and devices connected to them
- Allows easy access to the PCI/cPCI bus via the connectors
- Maintains a clean integration environment
- Supports a JTAG TAP connection through the PCI/cPCI bus interface or directly to the UUT
- Supports 3.3V, 5V and universal I/O PCI/cPCI cards
- Internal power supply included for powering up the Unit Under Test (UUT)
- Power indicator LEDs
- Selectable PCI bus clock speed
- Reset switch for generating reset to the UUT
- Software supplied contains BSDL and other files for automatic test pattern generation with the ScanPCI
- Compatible with the ScanPlus™ family of products for testing and in-system programming of Flash memories and CPLDs

Required hardware and software

The ScanPCI requires the following additional equipment that is sold separately and is not part of this product:

- Any of the Corelis Boundary-Scan Controllers. We recommend the high performance PCI-1149.1/Turbo with the ScanTAP-4 Intelligent Pod (please call Corelis for a list of other available controllers).
- ScanPlusTPG Software
- ScanPlus Runner Software
- Host PC computer, with the above products installed, as per the specific instructions found in these product's users manuals
- ScanPlus Merge Software (only required if testing CompactPCI cards)
- CompactPCI to PCI adapter (only required if testing CompactPCI cards)[1]

1. *Contact information for purchasing the CompactPCI to PCI adapter can be found in Chapter 5.*

Chapter 2
ScanPCI Installation

Installing and setting up the ScanPCI hardware. Connecting the UUT.

Product Components

The ScanPCI product package consists of the following components:

- ScanPCI Hardware
- ScanPCI User's Manual
- ScanPCI Software Disk

Please ensure that all materials listed are present and free from visible damage or defects before proceeding. If anything appears to be missing or damaged, contact Corelis at the number listed in the front of the manual immediately.

What's on the Disk

The disk contains the following test vector generation files:

Filename	Description
ScanPCI_3V.bsd	BSDL file for the 3.3V ScanPCI connector
ScanPCI_5V.bsd	BSDL file for the 5V ScanPCI connector
ScanPCI.top	An example topology file for the ScanPCI.
cPCI_adapter.net	Netlist for the CompactPCI to PCI adapter.
Compact_PCI_Board.sco	System Connection file for the CompactPCI to PCI adapter. Used by ScanPlus Merge to combine the netlists from the UUT and cPCI to PCI adapter.
ScanPCI_Selftest_inf.cvf	An infrastructure test for a ScanPCI with nothing connected to its PCI connectors and JP1 and JP2 installed. It is used with ScanPlus Runner as a basic self-test of the ScanPCI.

Table 2-1. Files on the Provided Software Disk

Connecting the Unit Under Test (UUT) to the ScanPCI

If the target UUT is designed to be a universal PCI card or to use 3.3 volts, install the card in the ScanPCI socket connector labeled *"**3.3V PCI**"*.

If the UUT is designed to use 5 volts, install the card in the ScanPCI socket connector labeled *"**5V PCI**"*.

Connecting to the Boundary-Scan Controller

There are two ways that the TAP from the target UUT can be connected to the boundary-scan controller. The method of connection depends on whether the TAP signals are brought to an external header or to the PCI card-edge connector.

Target UUT TAP Connections on an External Header

If the TAP signals from the target UUT are brought to a header, the recommended and most common approach to use an external ScanTAP-4 Intelligent Pod to chain the Target UUT with the ScanPCI module. Simply connect TAP1 from the pod to the TAP connector on the target UUT, and connect TAP2 from the pod to the ScanPCI connector labeled "TAP".

Figure 2-1 shows the TAP connections for the Target UUT on TAP1 and the ScanPCI module on TAP2.

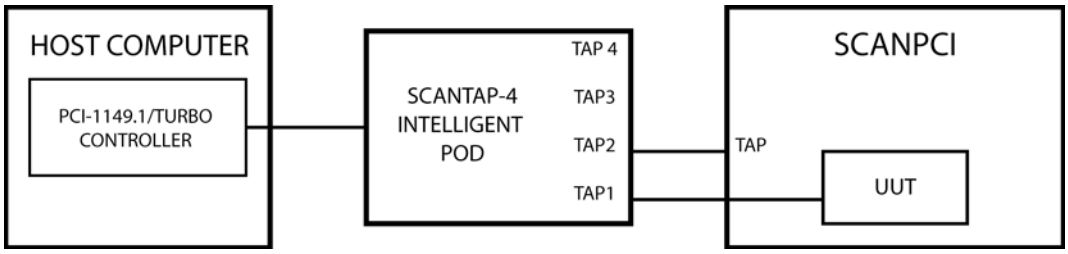

Figure 2-1. Connection of the ScanPCI and the Target using Separate TAPs

It is best to use a PCI-1149.1/Turbo equipped with a ScanTAP-4 Intelligent Pod, with one TAP connected to the ScanPCI and with additional TAP(s) connected to the UUT. However, any Corelis controller with an appropriate version of the Buffer-1149.1 can also be used to connect to the UUT and the ScanPCI on separate TAPs.

For this mode, both jumpers JP1 and JP2 should be installed.

An example of a UUT connected to the ScanPCI using a 2 TAP configuration is shown in Figure 2-2:

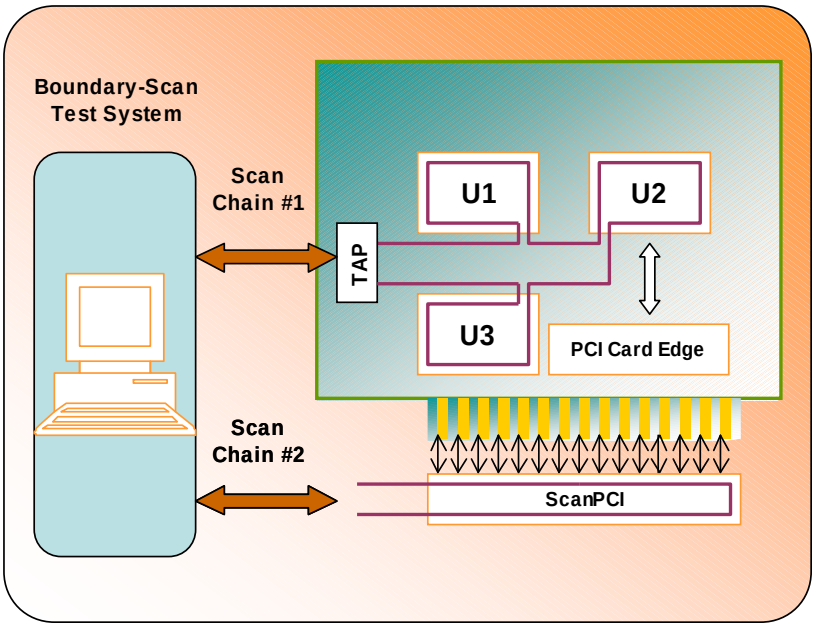

Figure 2-2. UUT Connection Example using Separate TAPs

Target UUT TAP Connections on the PCI Card-edge Connector

The ScanPCI also supports the connection of the TAP signals from the ScanPCI to the target UUT over the PCI card-edge connector. Connect the 10-pin cable from the boundary-scan controller (ScanTAP-4, Buffer-1149.1/Gang, etc.) to the ScanPCI TAP connector. The connection list for the TAP signals on the card-edge connector defined in the PCI specification must be followed.

Figure 2-3 shows a block diagram for the TAP connection from the ScanPCI module to the target UUT over the PCI card-edge connector.

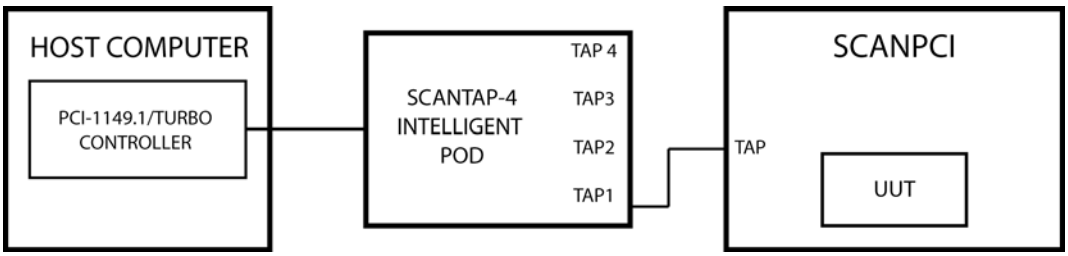

Figure 2-3. Block Diagram of the Connection to a ScanPCI with a Single TAP

For this mode, jumpers JP1 and JP2 need to be configured to jumper TDI to TDO across the ScanPCI connector that is not being used. For example, if a universal or 3.3V PCI card is being tested in the 3.3V PCI slot, then JP2 should be installed and JP1 should be open. If a 5V PCI card is being tested in the 5V PCI slot, then JP1 should be installed and JP2 should be open.

An example of a UUT connected to the ScanPCI using a single TAP configuration is shown in Figure 2-4:

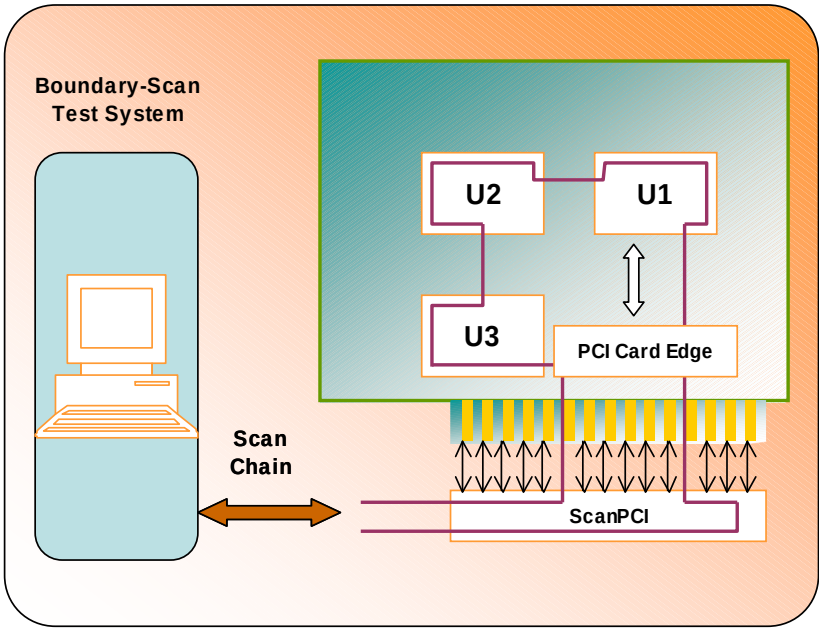

Figure 2-4. UUT Connection Example Using a Single TAP

Chapter 3
ScanPCI Hardware Reference

Connector Pinout, LEDs and Product Specification

Jumper Configuration

Four jumpers on the ScanPCI are used to configure the scan chain and the PCI clock. See Table 3-1.

When the TAP signals on the target UUT are present on the PCI card-edge connector, it is necessary to configure some jumpers to modify the ScanPCI scan chain. JP1 should be installed when testing 5V cards and removed when testing 3.3V cards. JP2 should be installed when testing 3.3V cards and removed when testing 5V cards. When the UUT TAP signals are brought to an external connector, both JP1 and JP2 should be installed.

If the target UUT requires a free running PCI clock for testing, a clock can be generated by placing a shunt across JP3. JP4 is used to configure the built-in oscillator that is used to provide the free running PCI clock. If the UUT requires a 33MHz clock signal, a shunt can be placed across pins 1 and 2 of JP4. If the UUT requires a 66MHz clock signal, a shunt can be placed across pins 2 and 3 of JP4. JP3 must be installed to enable the clock setting chosen by JP4.

Jumper	Signal	Description	Default
JP1	3.3V Slot Jumper	1-2: Jumpers TDI to TDO across the 3.3V PCI connector. This jumper should be removed when testing a 3.3V PCI card with the TAP signals on the PCI card-edge connector and installed when testing a 5V PCI card. JP1 should be installed when the TAP signals on the UUT are on an external header, no matter which voltage the card is.	installed
JP2	5V Slot Jumper	1-2: Jumpers TDI to TDO across the 5V PCI connector. This jumper should be removed when testing a 5V PCI card with the TAP signals on the PCI card-edge connector and installed when testing a 3.3V PCI card. JP2 should be installed when the TAP signals on the UUT are on an external header, no matter which voltage the card is.	installed
JP3	PCI Clock Enable	1-2: Enables a free running PCI clock open: Free running PCI clock is disabled	open
JP4	PCI Clock Select	1-2: Selects 33 MHz free running PCI Clock 2-3: Selects 66 MHz free running PCI Clock open: Built-in oscillators are disabled	open

Table 3-1. Jumper Configuration

TAP Connector Pinout

The TAP connector on the ScanPCI conforms to the popular Corelis 10-pin dual row (5x2) connector pinout. The pin assignment is standard, allowing any Corelis boundary-scan controller to connect to the ScanPCI using the appropriate 10-pin TAP cable.

Table 3-2 shows the pin assignments for the TAP connector.

Pin	Signal Name	I/O	Description
1	TRST*	In	TRST*
2	GND		Ground
3	TDI	In	Test Data In
4	GND		Ground
5	TDO	Out	Test Data Out
6	GND		Ground
7	TMS	In	Test Mode Select
8	GND		Ground
9	TCK	In	Test Clock
10	GND		Ground

Table 3-2. TAP Connector Connection List

Power Indicator LEDs

Two LEDs on the top of the ScanPCI unit, labeled **3.3V** and **5V**, illuminate when power is turned on.

Specifications

Size	10.5" x 9.0" x 4.5"
Status Indicators	Power ON/OFF indicator
Output Logic Levels	3.3V CMOS, 5V tolerant (see Table 3-3)
Input Logic Levels	TTL (see Table 3-3)
Maximum TCK clock frequency	10 MHz
JTAG TAP Connector	10-pin IDC (3M part no. 3793-6302 or equivalent).
JTAG Interface	IEEE-1149.1 compliant interface
Power	Internal ATX style power supply

Symbol	Conditions	Min	Max	Unit
V_{IH} High Level Input Voltage		1.7	5.75	V
V_{IL} Low Level Input Voltage		-0.5	0.8	V
V_{OH}	I_{OH} = -8mA DC	2.4		V
	I_{OH} = -0.1mA DC	3.1		V
V_{OL}	I_{OL} = 8mA DC		0.45	V
	I_{OL} = 0.1mA DC		0.2	V
I_I	$V_I = V_{cc}$ or GND	-10	10	µA
I_{OZ}	$V_o = V_{cc}$ or GND	-10	10	µA

Table 3-3. Signal Level Characteristics

ScanPCI Operating Characteristics

The following operating characteristics are not specifications, but are typical operating characteristics for the ScanPCI:

TEMPERATURE:	
Operating	0°C to +55° (+32°F to +131°F)
Non-operating	-40°C to +75°C (-40°F to +167°F)
ALTITUDE:	
Operating	up to 4600 meters (15,000 feet)
Nonoperating	up to 15,300 meters (50,000 feet)
Humidity	90% non-condensing. Avoid sudden extreme temperature changes that could cause condensation within the instrument.

Table 3-4. ScanPCI Operating Characteristics

Chapter 4
Preparation of Test Input Files

How to use the ScanPCI with the ScanPlus boundary-scan tools

Introduction

The ScanPCI integrates easily with a boundary-scan test plan. When a PCI card is installed in the PCI slot (socket) of the ScanPCI, the socket behaves like a boundary-scan component. Therefore, it is not normally necessary to make any changes to the netlist to include the ScanPCI in a test plan.

Once the PCI card is plugged into the socket of the ScanPCI, the boundary-scan test system will automatically test the PCI card-edge connector. However, regeneration of the interconnect tests (using ScanPlusTPG) with the relevant ScanPCI input files supplied on the floppy disk is required.

How to Generate Vectors using the ScanPCI

Copy **ScanPCI_3V.bsd** or **ScanPCI_5V.bsd** from the supplied disk to your design directory. Use ScanPCI_3V.bsd when testing universal or 3.3V PCI cards. Use ScanPCI_5V.bsd when testing 5V PCI cards.

The next step is to add the ScanPCI module to the topology file and regenerate your test vectors. In the topology file, the ScanPCI module takes the reference designator of the PCI card-edge connector from the schematic. Note that how the ScanPCI and target UUT are connected to the boundary-scan controller will determine the order that the components will appear in the topology file. If the ScanPCI unit is connected to TAP2 as recommended, then it is placed at the end of the topology file. If the ScanPCI unit is connected to TAP1, then it is placed at the beginning of the topology file.

The next page shows an example topology file that describes a target system with a PCI card installed in the 3.3V PCI slot of a ScanPCI. The two TAPs are chained together with a ScanTAP-4. Figure 4-1 shows the UUT's topology file before the ScanPCI module is added. The modified topology file with the ScanPCI module (connected to TAP 2) added is shown in Figure 4-2.

Note: In certain cases it may be required to modify the netlist because some schematic capture programs use a separate reference designator for the front and back of the PCI card-edge connector (example: P1CS1 and P1SS1). If this is the case, the easiest solution is to search for one reference designator and replace all cases of it with the other.

```
!-------------------------------------------------
!  Boundary-Scan Chain Topology File
!-------------------------------------------------

CHAIN   chain1
        DEVICES

!     ------   ------------------   ----------   -------
!     DEVICE   BSDL FILE ------->   PACKAGE ->   BYPASS?
!     ------   ------------------   ----------   -------
      U1       "xc18v04_vq44.bsd"   vq44         NO
      U2       "xc2s200_fg456.bsd"  FG456        NO
      U3       "xc2s200_fg456.bsd"  FG456        NO
!     ------   ------------------   ----------   -------

        END_DEVICES
END_CHAIN
```

Figure 4-1. Example Topology *.top File Before the ScanPCI is Added

```
!-------------------------------------------------
!  Boundary-Scan Chain Topology File
!  Example for the ScanPCI
!-------------------------------------------------

CHAIN   chain1
        DEVICES

!     ------   ------------------   ----------   -------
!     DEVICE   BSDL FILE ------->   PACKAGE ->   BYPASS?
!     ------   ------------------   ----------   -------
      U1       "xc18v04_vq44.bsd"   vq44         NO
      U2       "xc2s200_fg456.bsd"  FG456        NO
      U3       "xc2s200_fg456.bsd"  FG456        NO

      P1CS1    "ScanPCI_3V.bsd"     PCI_CONN     NO
!     ------   ------------------   ----------   -------

        END_DEVICES
END_CHAIN
```

Figure 4-2. Example Topology *.top File After the ScanPCI is Added

Chapter 5
Testing CompactPCI Cards

How to use the ScanPCI with the ScanPlus boundary-scan tools to test CompactPCI Cards

Introduction

With the use of a CompactPCI to PCI adapter, the ScanPCI can easily be used to test CompactPCI (cPCI) cards. A cPCI to PCI adapter is available from Twin Industries (www.twinhunter.com). The following table lists the part number for the adapter at the time that this manual was printed. Note that there may be other manufacturers that offer similar parts as well:

Twin Industries Part Number	***Description***
2000-64PCI	cPCI to PCI Passive Adapter

Once the cPCI card is plugged into the socket of the ScanPCI (via the cPCI to PCI adapter), the boundary-scan test system will automatically test the cPCI card-edge connector. However, regeneration of the interconnect tests (using ScanPlusTPG) with the relevant ScanPCI input files supplied on the floppy disk is required. Regeneration of the files consists of three main steps:

1. Use ScanPlus Merge to combine the netlist of the CompactPCI to PCI Adapter with the UUT.
2. Modify the topology file to add the ScanPCI module.
3. Regenerate the test vector files using ScanPlusTPG.

Merging the CompactPCI Adapter and the UUT

ScanPlus Merge is required to combine the netlists of the UUT and the CompactPCI Adapter. Follow the instructions in the ScanPlus Merge User's Manual to install ScanPlus Merge if it has not already been installed. To merge the two assemblies, follow the steps below.

Step 1 – Starting ScanPlus Merge

ScanPlus Merge can be started by selecting the **ScanPlus Merge** entry from the Windows Start menu. When ScanPlus Merge starts, the main window is displayed as shown in Figure 5-1.

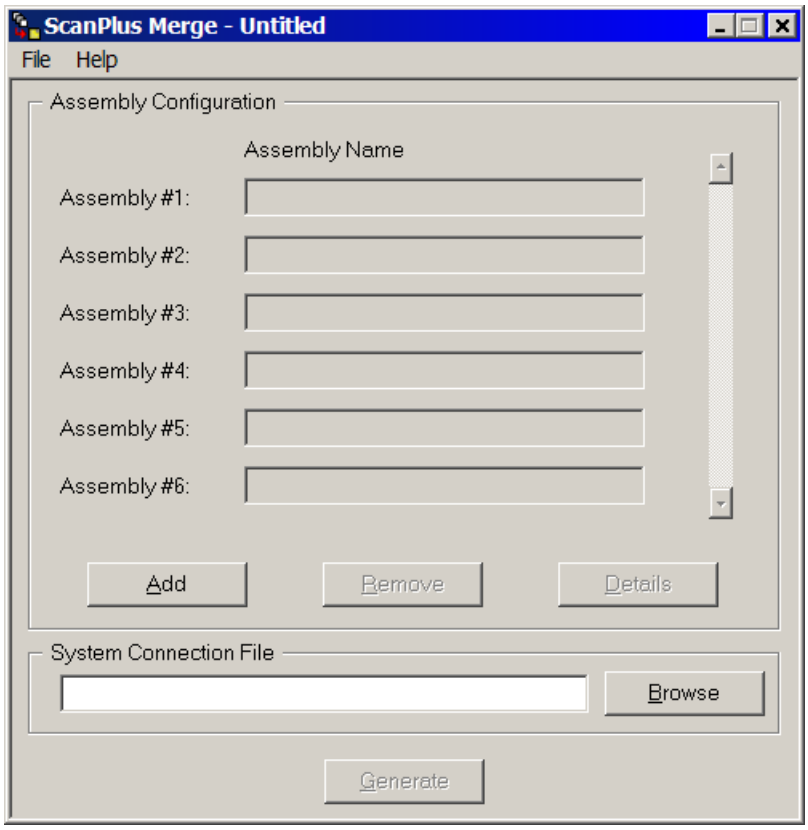

Figure 5-1. ScanPlus Merge Main Window

Step 2 – Add the Unit Under Test (UUT) Assembly

Since the UUT is the first target in the scan chain, it will be added first. Click on the **Add** button to add a new assembly to the current Merge Plan. A new assembly will be added and the default name of "ASSEMBLY1" will appear in the first assembly entry as shown in Figure 5-2.

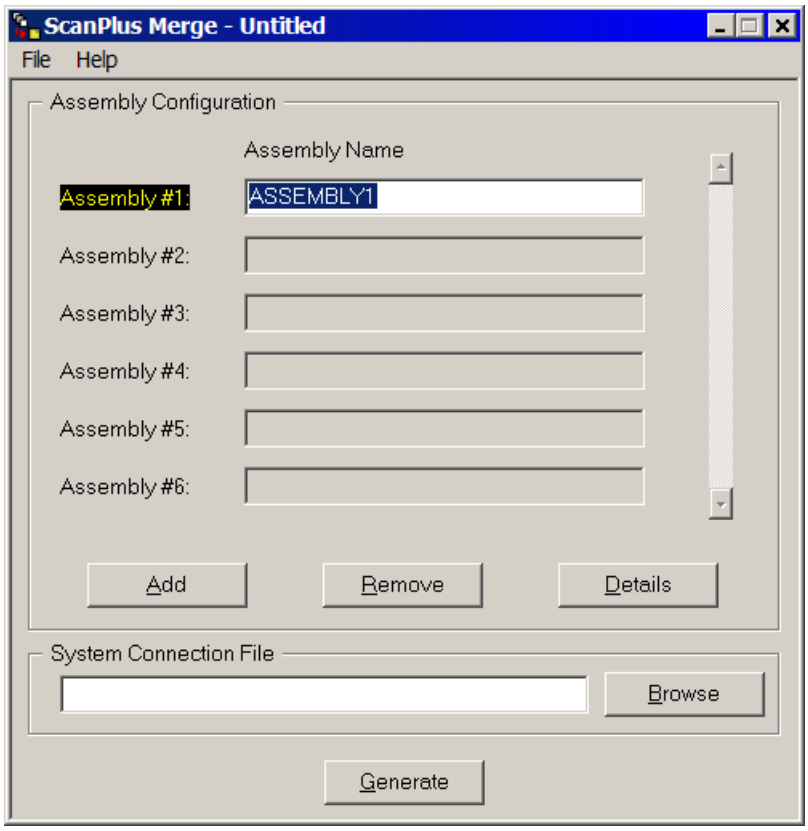

Figure 5-2. ScanPlus Merge Main Window with a New Assembly

Give the new assembly entry for the UUT a meaningful name by typing it into the Assembly #1 name field. Your screen should now look similar to Figure 5-3.

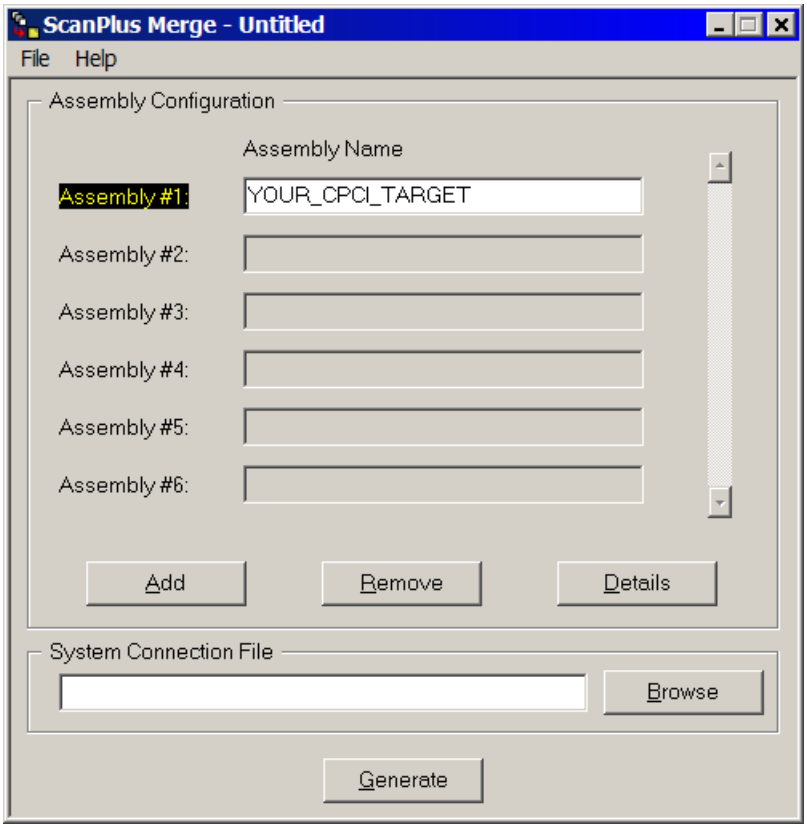

Figure 5-3. ScanPlus Merge Main Window Showing Renamed UUT Assembly

Double click on the UUT assembly name or click on the **Details** button to bring up the Assembly Details screen for the UUT assembly. This screen, shown in Figure 5-4, is where the Test Step files are entered for the UUT assembly.

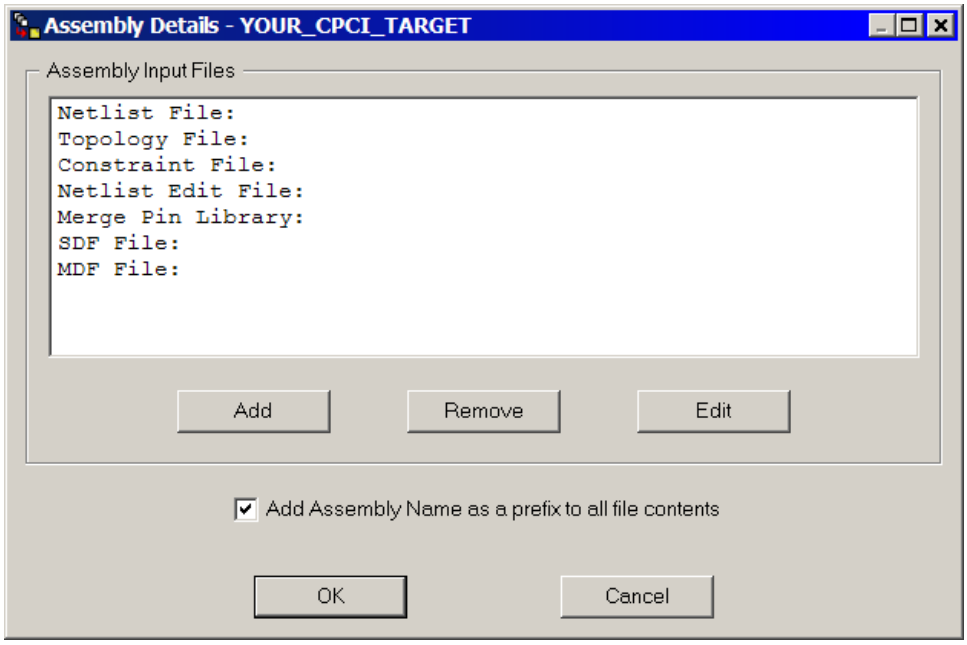

Figure 5-4. Assembly Details Window for the UUT Assembly

Click on the first row "Netlist File". This will select the **Netlist File** row as shown in Figure 5-5.

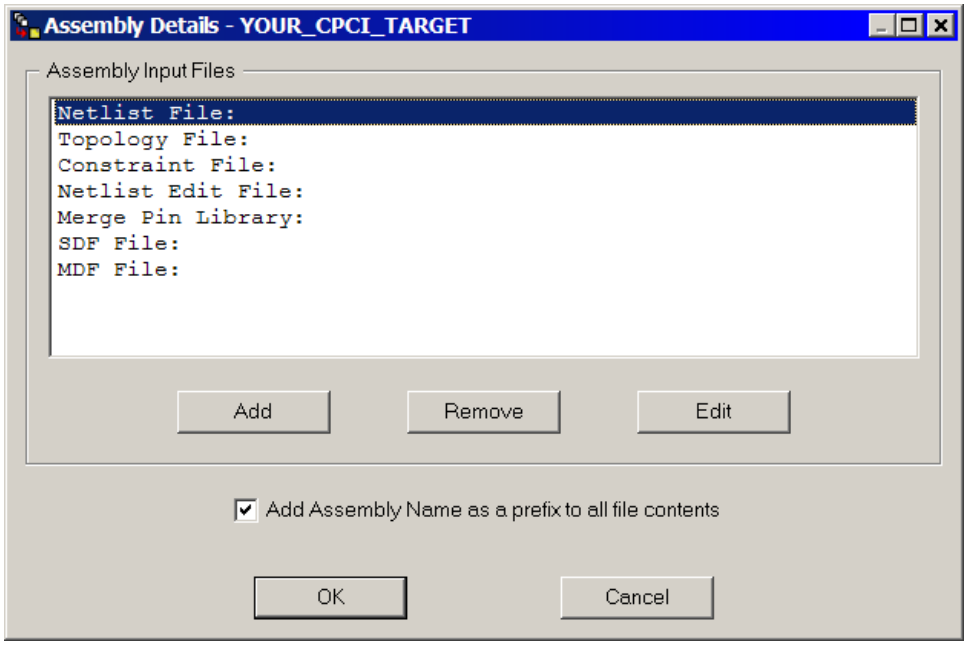

Figure 5-5. Assembly Details Window with Netlist File Row Selected

Click on the **Add** command button. A new **Add Files to Assembly** file browser window will be displayed. Select the netlist for the UUT and click on the **Add** command button. The Assembly Details screen will be displayed again and will include the netlist file. Resize the window so that the entire pathname is visible, and your screen should look like Figure 5-6.

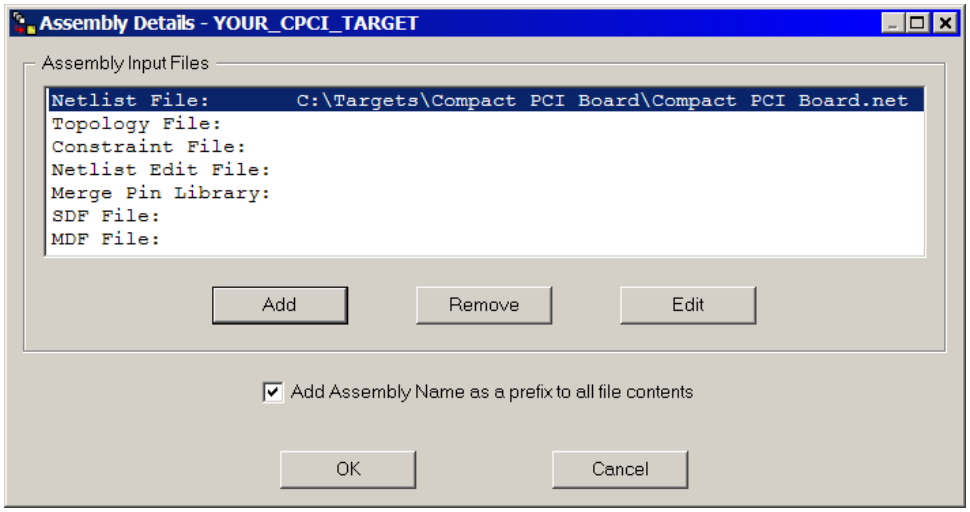

Figure 5-6. UUT Netlist File Selected

Click on the second row labeled **Topology File**. This will select the **Topology File** row. Click on the **Add** command button and a new **Add Files to Assembly** file browser window is displayed. Select the topology file for the UUT and click on the **Add** command button. The Assembly Details screen will be displayed again and will include the topology file as shown in Figure 5-7. Add the constraint, netlist edit, merge pin library SDF and MDF files (if any) to the assembly in the same way. The configuration of the UUT assembly is now complete. Click on the **OK** button to return to the main screen.

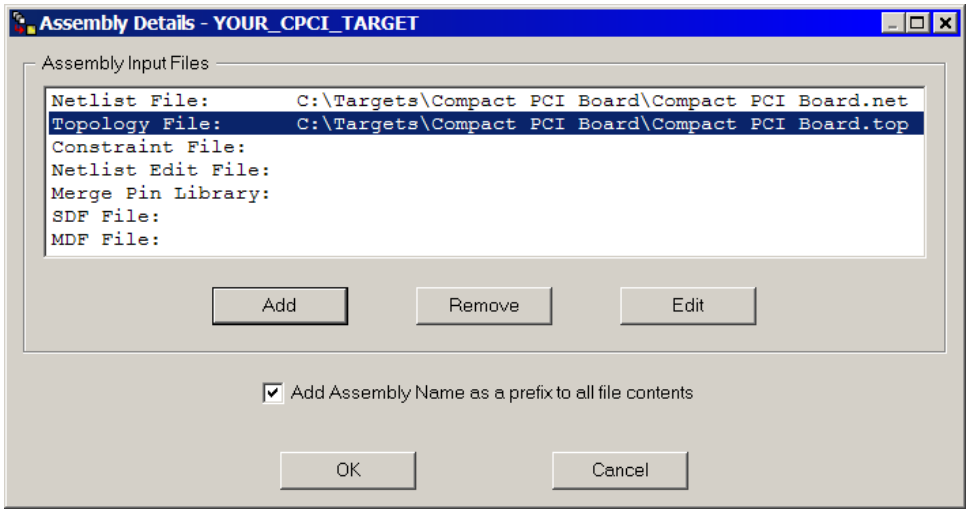

Figure 5-7. UUT Topology File Selected

Step 3 – Add the CompactPCI Adapter Assembly

Click on the **Add** button to add a new assembly to the current configuration. A new assembly will be added and the default name of "ASSEMBLY2" will appear in the second assembly entry as shown in Figure 5-8.

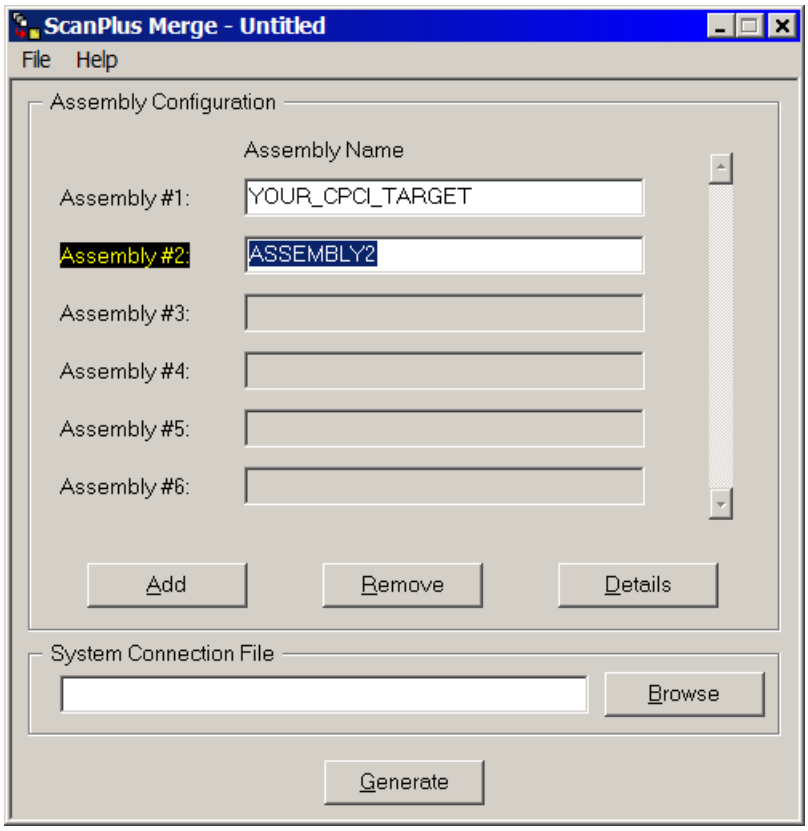

Figure 5-8. ScanPlus Merge Main Window with a Second Assembly Added

Give the new assembly entry for the CompactPCI Adapter a meaningful name by typing "CPCI_ADAPTER" into the Assembly #2 name field. Your screen should now look similar to Figure 5-9.

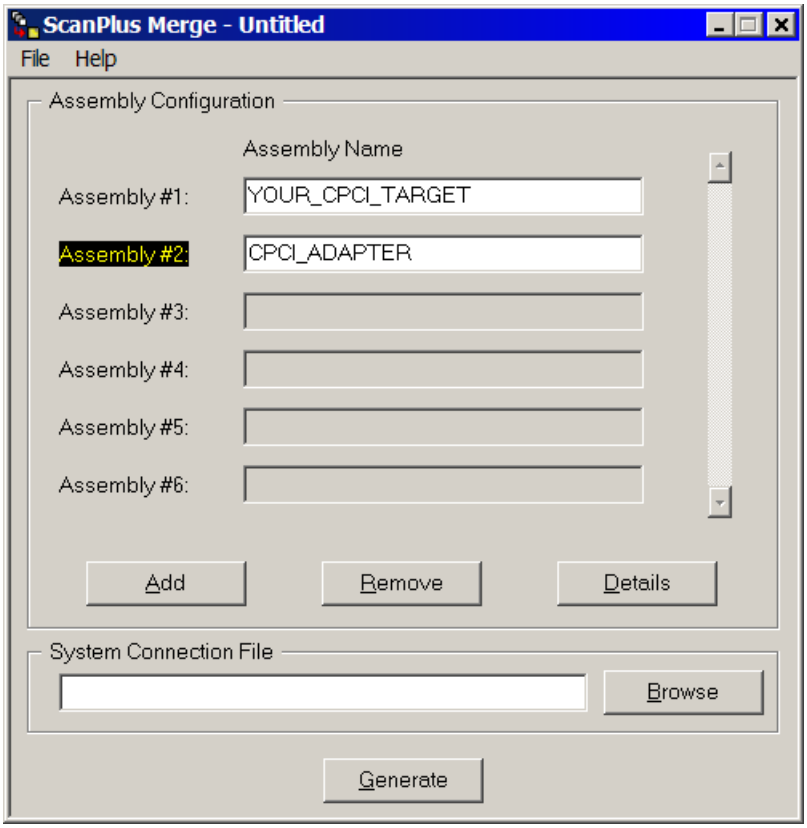

Figure 5-9. ScanPlus Merge Main Window Showing Renamed Assembly

Double click on the CPCI_ADAPTER assembly name or click on the **Details** button to bring up the Assembly Details screen for the new assembly. This screen, as shown in Figure 5-10, is where the Test Step files are added to the assembly.

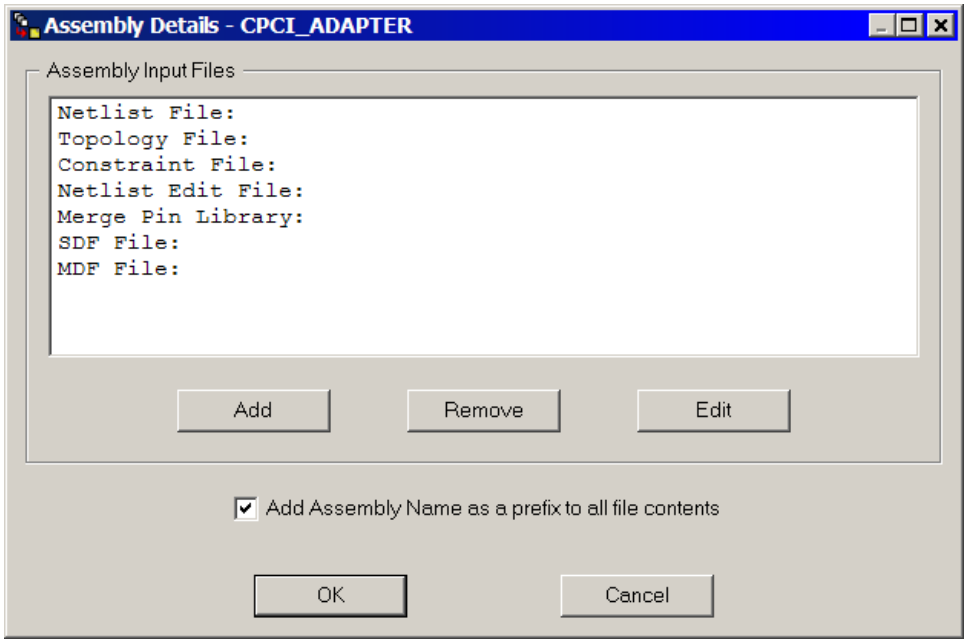

Figure 5-10. Assembly Details Window

Since there are no boundary-scan components on the CompactPCI to PCI adapter, only a netlist is required. Add the adapter netlist to the assembly as shown previously, your screen should look similar to Figure 5-11. The configuration of the second assembly is now complete. Click on the **OK** button to return to the main window.

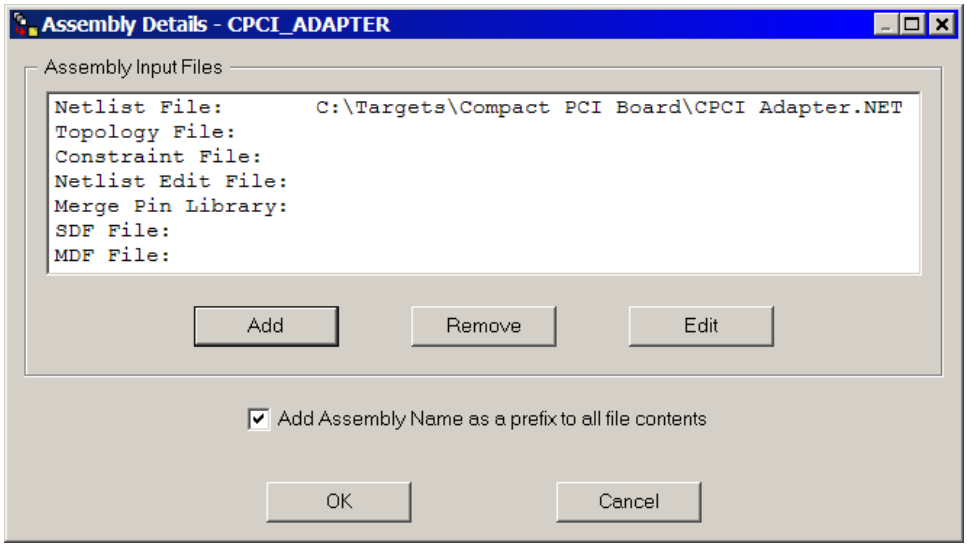

Figure 5-11. Assembly Details after Test Step files added

Step 4 – Add the System Connection File

The System Connection file, shown in Figure 5-12, describes the interconnections between the defined assemblies.

```
! System Connection File for merging the Compact
! PCI Adapter with your Compact PCI target

CONNECTIONS

        YOUR_CPCI_TARGET J1     CPCI_ADAPTER P2

        YOUR_CPCI_TARGET J2     CPCI_ADAPTER P3


END_CONNECTIONS

! Replace the string "YOUR_CPCI_TARGET" with the assembly name
! used for your target in ScanPlus Merge.  Replace the reference
! designators J1 and J2 with the reference designators of the
! compact PCI connectors in your target.
```

Figure 5-12. System Connection File

To add the System Connection file to the Merge Plan, click on the **Browse** button in the System Connection File area near the bottom of the main window and a file browsing window will appear. Select the file **CompactPCI Board.sco** and click on the **Open** button.

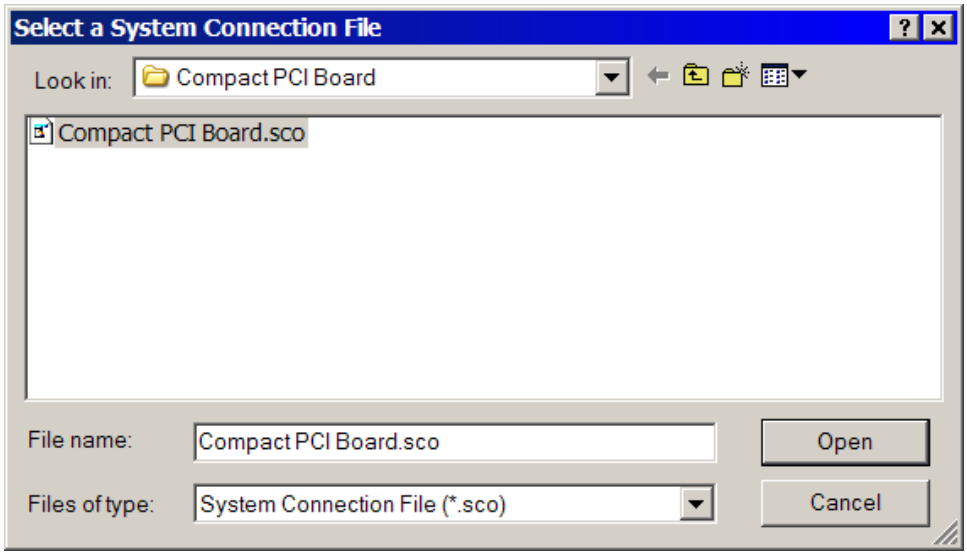

Figure 5-13. System Connection File Browsing Window

The ScanPlus Merge main window will now be displayed as shown in Figure 5-14. The Merge Plan is now complete.

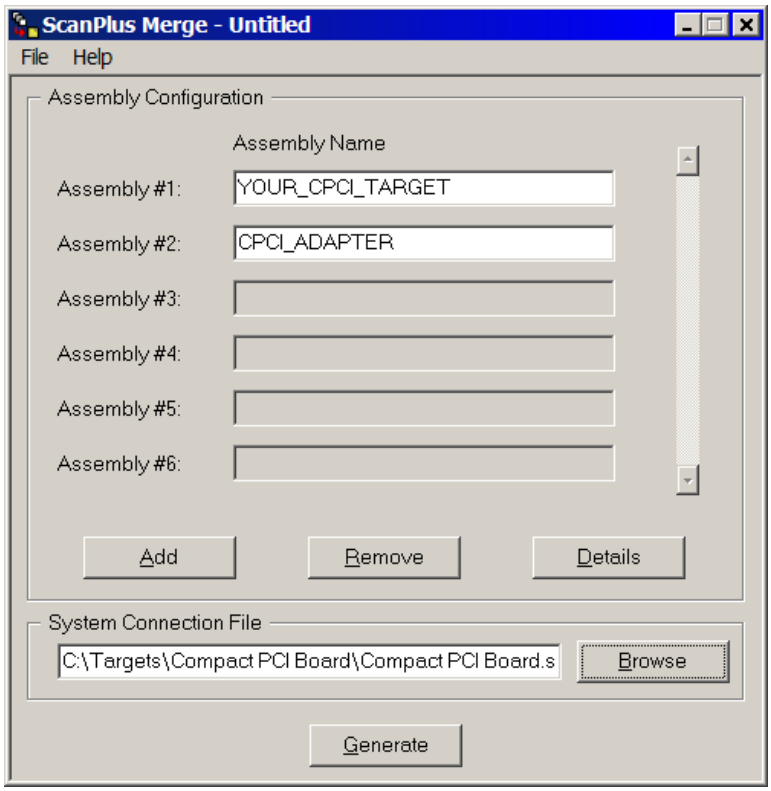

Figure 5-14. ScanPlus Merge Main Window with System Connection File

Step 5 – Merge the Assemblies

Click on the **Generate** button to begin the merging process. Because this is a new unsaved Merge Plan, the **Save Merge Plan File** window will be displayed. Move to the directory where you would like the merged test plan files to be stored and type in a meaningful Merge Plan filename like "Your_Target_with_ScanPCI". Your window should now look similar to Figure 5-15. Click on the **Save** button and the Merge Plan settings will be saved to the file that you specified and the merge process will begin. All files generated by the merge process will be stored in the same directory as the ".mpf" Merge Plan file.

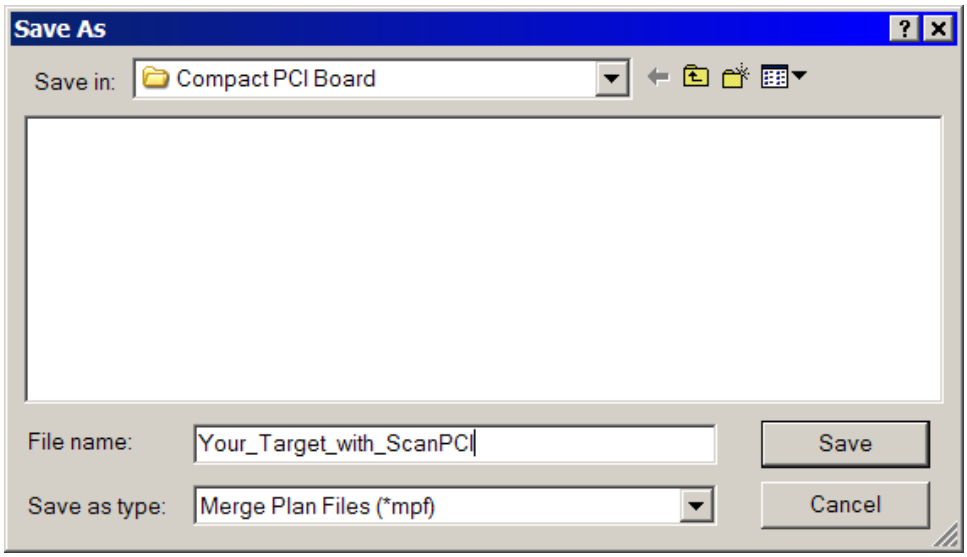

Figure 5-15. Saving the Merge Plan file

The Merge Status window will appear and provide ongoing status of the assembly merging process. Part of the merge process involves copying the BSDL files, cluster Signal Level (SLF) files, and memory cluster Memory Information (MIF) files for each assembly to the merged target directory. When ScanPlus Merge detects duplicate files, a **Confirm File Replace** window will appear as shown in Figure 5-16. For this tutorial, click on the **Yes to All** button which will cause ScanPlus Merge to automatically overwrite all duplicate files without asking.

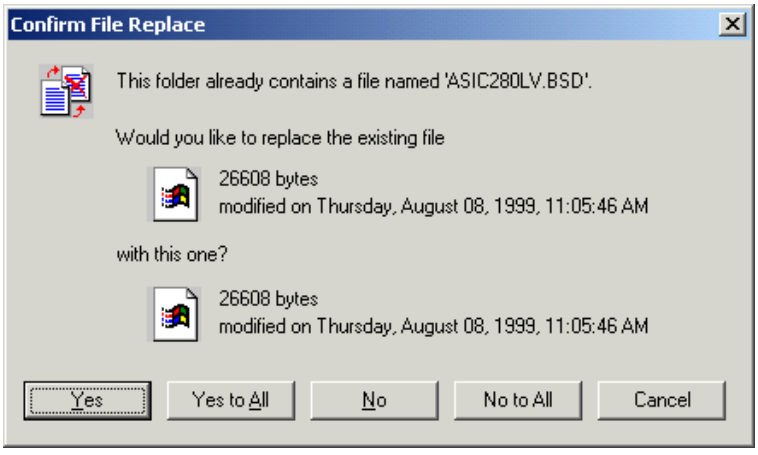

Figure 5-16. Confirm File Replace Window

When the merge process is complete as shown in Figure 5-17, click on the **OK** command button to close the Merge Status window. The main ScanPlus Merge window will then be displayed again.

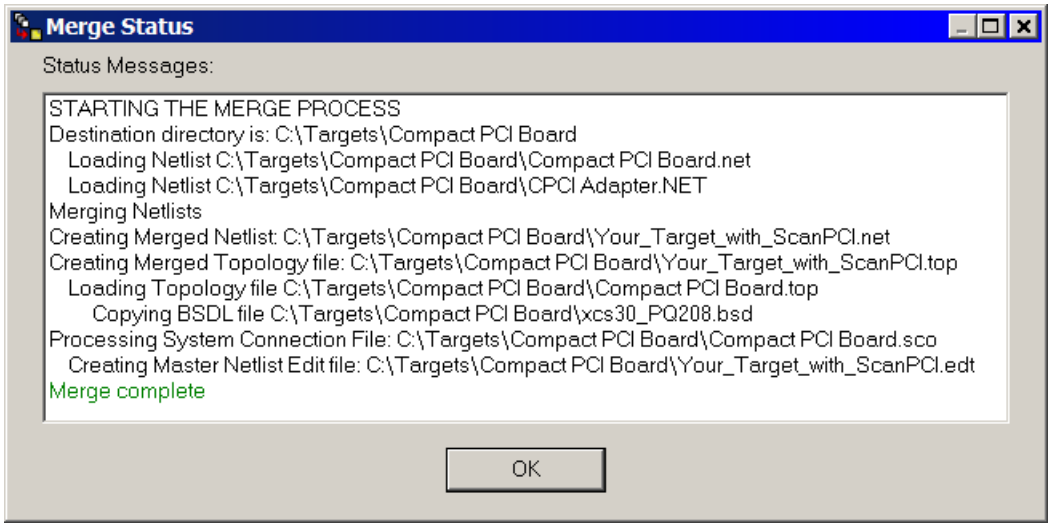
Merge Status
Status Messages:
STARTING THE MERGE PROCESS
Destination directory is: C:\Targets\Compact PCI Board
Loading Netlist C:\Targets\Compact PCI Board\Compact PCI Board.net
Loading Netlist C:\Targets\Compact PCI Board\CPCI Adapter.NET
Merging Netlists
Creating Merged Netlist: C:\Targets\Compact PCI Board\Your_Target_with_ScanPCI.net
Creating Merged Topology file: C:\Targets\Compact PCI Board\Your_Target_with_ScanPCI.top
Loading Topology file C:\Targets\Compact PCI Board\Compact PCI Board.top
Copying BSDL file C:\Targets\Compact PCI Board\xcs30_PQ208.bsd
Processing System Connection File: C:\Targets\Compact PCI Board\Compact PCI Board.sco
Creating Master Netlist Edit file: C:\Targets\Compact PCI Board\Your_Target_with_ScanPCI.edt
Merge complete
OK

Figure 5-17. Merge Status Window Indicating Completion

When the merge process is complete, all of the resulting files are placed in the directory where the Merge Plan file (*.mpf) was saved. Table 5-1 shows a list of all files created by the merge process.

Required Files	Description
*.bsd	BSDL file(s) which describe the boundary-scan components.
Your_Target_with_ScanPCI.net	This file contains the merged netlists of the UUT and the CompactPCI Adapter. It will be named after the Merge Plan file.
Your_Target_with_ScanPCI.top	This file contains the merged topology files of the UUT and the CompactPCI Adapter. It will be named after the Merge Plan file.
Your_Target_with_ScanPCI.con	This file contains the merged constraint files of the UUT and the CompactPCI Adapter. It will be named after the Merge Plan file.
Your_Target_with_ScanPCI.edt	This file contains the merged netlist edit files of the UUT and the CompactPCI Adapter. It will be named after the Merge Plan file.

Table 5-1. Files Created by the Merge Process

Modifying the Topology File to Include the ScanPCI

The assembly merging process is now complete but the topology file needs to be modified to include the ScanPCI in the scan chain.

Copy **ScanPCI_3V.bsd** or **ScanPCI_5V.bsd** from the supplied disk to your design directory. Use ScanPCI_3V.bsd when testing universal or 3.3V cPCI cards. Use ScanPCI_5V.bsd when testing 5V cPCI cards.

The next step is to add the ScanPCI module to the topology file and regenerate your test vectors. In the topology file, the ScanPCI module takes the reference designator of the cPCI to PCI adapter card-edge connector J1. Note that how the ScanPCI and target UUT are connected to the boundary-scan controller will determine the order that the components will appear in the topology file. If the ScanPCI unit is connected to TAP2 as recommended, then it is placed at the end of the topology file. If the ScanPCI unit is connected to TAP1 then it is placed at the beginning of the topology file.

On the next page is an example of a topology file that describes a target system with a PCI card installed in the 3.3V PCI slot of a ScanPCI. The two TAPs are chained together with a ScanTAP-4. Figure 4-1 shows the UUT's topology file before the ScanPCI module is added. The modified topology file with the ScanPCI module (connected to TAP 2) added is shown in Figure 4-2. Note how the reference designators in the topology file are prefixed by the assembly name from ScanPlus Merge.

The merged test generation files may then be compiled into test vectors with ScanPlus TPG as usual.

```
!-------------------------------------------------
!  Boundary-Scan Chain Topology File
!  Example for the ScanPCI
!-------------------------------------------------

CHAIN   chain1
        DEVICES

! ---------------  ------------------   ----------  -------
!    DEVICE        BSDL FILE ---->      PACKAGE ->  BYPASS?
! ---------------  ------------------   ----------  -------
  cPCI_Target_U1   "xc18v04_vq44.bsd"   vq44        NO
  cPCI_Target_U2   "xc2s200_fg456.bsd"  FG456       NO
  cPCI_Target_U3   "xc2s200_fg456.bsd"  FG456       NO
! ---------------  ------------------   ----------  -------

        END_DEVICES
END_CHAIN
```

Figure 5-18. Example Topology *.top File Before the ScanPCI is Added

```
!-------------------------------------------------
!  Boundary-Scan Chain Topology File
!  Example for the ScanPCI
!-------------------------------------------------

CHAIN   chain1
        DEVICES

! ---------------  ------------------   ----------  -------
!    DEVICE        BSDL FILE ---->      PACKAGE ->  BYPASS?
! ---------------  ------------------   ----------  -------
  cPCI_Target_U1   "xc18v04_vq44.bsd"   vq44        NO
  cPCI_Target_U2   "xc2s200_fg456.bsd"  FG456       NO
  cPCI_Target_U3   "xc2s200_fg456.bsd"  FG456       NO

  CPCI_ADAPTER_P1  "ScanPCI_3V.bsd"     PCI_CONN    NO
! ---------------  ------------------   ----------  -------

        END_DEVICES
END_CHAIN
```

Figure 5-19. Example Topology *.top file After the ScanPCI is Added

Chapter 6
Executing Selftest with ScanPlus Runner

How to run a basic sanity check on the ScanPCI unit

ScanPlus Runner (sold separately) can load and run the compact vector file, ScanPCI_Selftest_inf.cvf, and quickly verify that the ScanPCI is functional. Both the ScanPlus Runner software and a Corelis Boundary-Scan controller such as the PCI-1149.1/Turbo are required to execute this file.

Infrastructure Test

The infrastructure test verifies the TAP connection between the controller and the ScanPCI. The infrastructure test requires a Corelis boundary-scan controller, a 10-pin TAP cable from the controller and a ScanPCI unit. The following steps execute an infrastructure test.

Step 1 Remove any PCI cards from the ScanPCI's PCI test sockets.

Step 2 Verify that JP1 and JP2 are installed.

Step 3 Connect the 10-pin TAP cable from the external controller to the TAP connector of the ScanPCI.

Step 4 Apply power to the ScanPCI.

Step 5 Make sure that both LEDs on the ScanPCI illuminate.

Step 6 Double-click on the ScanPlus Runner Icon on the Host PC.

Step 7 Select New Test Plan from the File menu and click on the Add button.

Step 8 With the file browser, find and select the **ScanPCI_Selftest_inf.cvf** file. Click OK.

Step 9 Select Controller from the Setup menu, then choose the appropriate Boundary-Scan controller and set the frequency to 1 MHz and the TAP voltage to 3.3V. Make sure that the controller is configured to use TAP 1.

Step 10 Select Run Test. The test should run and pass. Figure 6-1 shows a passing infrastructure test.

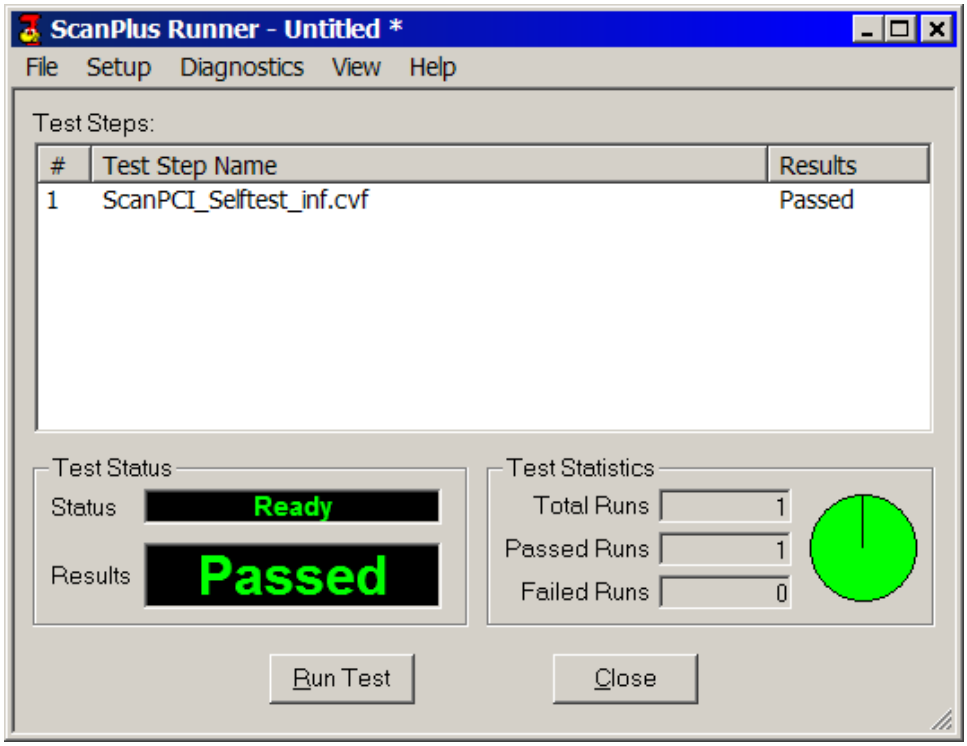

Figure 6-1. ScanPlus Runner Infrastructure Test